IN THE CLAIMS

Please cancel claims 19-27 without prejudice.

1. [Currently amended] A process of forming an optical subassembly in an integrated circuit, the process comprising:

defining electrically conducting lines and bonding pads in a metallization layer on a substrate;

depositing a passivation layer over said metallization layer;

etching said passivation layer to remove said passivation layer from each of said bonding pads and a portion of said metallization layer ~~associated~~ corresponding with each of said bonding pads;

diffusing Cr from said lines proximate said bonding pads to prevent solder wetting down lines;

bonding an optical device to one of said bonding pads; and

attaching said substrate to a carrier utilizing solder bond attachment.

2. [Currently amended] The process according to claim 1 further comprising:

obtaining a carrier having a cavity on a first side of said carrier, said cavity configured to provide clearance for said optical device ~~depending from~~ bonded to said substrate; and

attaching a mini ball grid array (mini-BGA) on said first side.

3. [Original] The process according to claim 2 further comprising attaching a ball grid array (BGA) on a second side of said carrier for subsequent mounting of said optical subassembly.

4. [Original] The process according to claim 3 further comprising:

aligning said mini-BGA of said carrier with a portion of said bonding pads designated to receive said mini-BGA on said substrate; and

joining said carrier to said substrate utilizing a fluxless process to keep said optical device clean.

5. [Original] The process according to claim 1, wherein subsequent attaching components to the subassembly utilizes a temperature hierarchy to prevent movement of said optical device relative to said substrate, and said substrate relative to said carrier when said subassembly is heated for said subsequent attaching.

6. [Original] The process according to claim 1, wherein said bonding pads allow for wire bond attachment and solder bond attachment.

7. [Currently amended] The process according to claim 1, wherein said forming of said metallization layer comprises:

depositing a first Cr layer on said substrate;

depositing a Cu layer on said first Cr layer;

depositing a Ni layer on said Cu layer;

depositing a Au layer on said Ni layer; and

depositing a second Cr layer on said Au layer.

8. [Original] The process according to claim 7, wherein the first Cr layer thickness is about 200 to about 800 Å (angstroms), the Cu layer thickness is about 3 to about 5 μM (microns), the Ni layer thickness is about 2 to about 4 μM (microns), the Au layer thickness is about 0.4 to about 0.7 μM (microns), and the second Cr layer thickness is about 500 to about 1000 Å (angstroms).

9. [Original] The process according to claim 7, wherein said portion of metallization layer removed is said second Cr layer.

10. [Original] The process according to claim 1, wherein said passivation layer comprises a material selected from the group consisting of a SiO_2, Si_3Ni_4, polyimide dielectrics and mixtures thereof.

11. [Original] The process according to claim 1, wherein said passivation layer has a thickness of about 2000 to about 3000 Å (angstroms) when SiO_2 or Si_3Ni_4 is utilized.

12. [Original] The process according to claim 1, wherein said passivation layer has a thickness of about 2 to about 4 μM (microns) when polyimide is utilized.

13. [Original] The process according to claim 2, wherein said mini ball grid array (mini-BGA) on either side of said cavity includes solder balls having a melting point of about 240°C .

14. [Original] The process according to claim 13, wherein said joining said carrier to said substrate includes reflowing of said solder balls by a fluxless process.

15. [Original] The process according to claim 14, wherein said fluxless process includes one of:

reflowing in H_2 gas , and

ionizing fluorinated gases in a plasma chamber and reacting with Sn-rich surfaces to enhance wetting of molten Sn-rich solder to said bonding pads on said SiOB.

16. [Original] The process according to claim 3, wherein said BGA include solder balls having a melting point of about 183°C.

17. [Original] The process according to claim 1, wherein said one of said bonding pads for said optical device comprises an area array of flip-chip bond pads.

18. [Original] The process according to claim 2, wherein surface mount technology (SMT) devices are mounted on said first side of said carrier.

19 - 27. [Canceled]